

**Comparing Various Backside Power Delivery Schemes:** As semiconductor technology scaling continues, it becomes more challenging to fabricate low-loss power delivery networks (PDNs). Backside power delivery architectures have been introduced and are being developed for advanced nodes to mitigate the increasing risks of both static IR-drop (SIR) and dynamic voltage drop (DvD) that occur with conventional front-side PDNs. Samsung researchers will describe how three different backside power delivery schemes under development industry-wide compare to front-side power delivery performance: 1) through-silicon vias; 2) buried power rails; and 3) back-side direct contacts. These differ in how the backside power delivery network is connected to active devices. The Samsung researchers also will describe the importance of system-level analysis and design co-optimization between the on-chip PDN and the packaging.

The schematic above shows frontside and backside power delivery architectures.

**(Paper 22.3, “*System-Level Analysis and Design Optimization of Back-side Power Delivery Network for Advanced Nodes*,” K. Song et al, Samsung)**